REMARKS

Claims 6-9, 11-13 and 15-19 are pending in the present application. Claims 6, 11, and 16 have been amended. Claim 14 has been canceled.

Claim Rejections-35 U.S.C. 112

Claims 6-9 and 11-19 have been rejected under 35 U.S.C. 112, first paragraph, as allegedly failing to comply with the written description requirement. The Examiner has asserted that the claimed feature "whereby edges of said protective layer are not covered by sidewall spacers", is not described in the specification in such a way as to reasonably convey that the inventor, at the time the application was filed, had possession of the claimed invention. This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

As emphasized on page 7 of the Amendment dated July 22, 2005, Manual of Patent Examining Procedure Section 2163 sets forth the principle that it is well accepted that a satisfactory description may be in the claims **or any other portion of the originally filed specification**. As the court held in *Lockwood v. American Airlines, Inc.*,(107 F.3d 1565, 1572, 41 USPQ2d 1961, 1966 (Fed. Circ. 1997): "An Applicant shows possession of the claimed invention by describing the claimed invention with all of its limitations using such descriptive means as words, structures, figures, diagrams, and formulas that fully set forth the claimed invention."

As further set forth in MPEP section 2163:

"**Possession** may be shown in a variety of ways including description of an actual reduction to practice, or by showing that the invention was "ready for patenting" such as **by the disclosure of drawings** or structural chemical formulas that show the invention was complete, or by describing distinguishing identifying characteristics sufficient to show that the applicant was in possession of the claimed invention" (our emphasis added).

Accordingly, as asserted in the Amendment dated July 22, 2005, Applicant respectfully submits that at least in view of Fig. 1(h), the original application reasonably conveys possession of the above noted features, whereby "edges of said protective layer are not covered by sidewall spacers". Accordingly, claims 6-9 and 11-19 as pending in view of the Amendment dated July 22, 2005, should thus be considered as in compliance with 35 U.S.C. 112, first paragraph.

On page 3 of the Final Office Action dated August 9, 2005, the Examiner asserted that "Since the drawing is only an illustration of the invention, a limitation of the claim must have support in the original specification".

Applicant respectfully submits that the above noted position as taken by the Examiner is in direct contradiction to the above noted portions of MPEP section 2163 and the *Lockwood v. American Airlines, Inc.* decision. Clearly, it is well settled that the drawings are part of the original specification. Moreover, as clearly set forth in MPEP section 2163, disclosure in drawings is sufficient to show possession of a claimed invention.

With further regard to this rejection, as described on page 3 of the present application with respect to Fig. 2(e), oxide layer 36 is deposited on the structure at a thickness enough to obtain a sidewall length in order to form sidewalls. Thereafter, oxide layer 36 is anisotropically etched to form sidewalls 37 as shown in Fig. 2(f). However, because of non-uniformities in oxide layer 36 as well as in the speed of the anisotropic etching process, an overeteching process must be performed to completely remove oxide layer 36 from on gate 35 and from on substrate 31, so that sidewalls 37 remain only on gates 35. However, the problem with this conventional process is that the overetching necessary to completely remove oxide layer 36 undesirably thins field oxide layer 34. This decreases isolating voltage of field oxide layer 34, so that inter-device leakage current is increased.

Accordingly, it should be understood that an object of the present invention is to provide a structure whereby a deposited oxide layer used to form a sidewall is completely removed from on a gate and from on the corresponding substrate by overetching, without thinning a field oxide layer. This is accomplished by providing a protective layer on the field oxide. As may be readily understood in view of Fig. 1(h) of the present application, a structure having sidewalls 37 on gates 35 and a protective layer 12 on field oxide layer 34 is provided. Oxide layer 36 is completely removed from the structure, except for remaining on sidewalls 37 of gates 35.

Applicant respectfully submits that one of ordinary skill would readily understand that the present application as noted above reasonably conveys that the inventor, at the

time the application was filed, had possession of the invention as claimed pending in view of the Amendment dated July 22, 2005. That is, the application reasonably conveys a structure including sidewalls on side surfaces of a gate, and not on side surfaces of a protective layer formed on a field oxide layer. Applicant respectfully submits that claims 6-9 and 11-19 pending in view of the Amendment dated July 22, 2005, are thus in compliance with 35 U.S.C. 112, first paragraph, for at least these additional resons.

Although it is Applicant's position that the rejection under 35 U.S.C. 112, first paragraph, is improper for at least the above noted reasons, independent claim 6, 11 and 16 have been respectively amended in view of the Examiner's concerns, merely for the purpose of advancing prosecution of this application. For instance, the semiconductor device of claim 6 has been amended to include in combination "sidewall spacers of silicon oxide film formed on the side surfaces of said first and second gates, and not on the side surfaces of said protective layer". Claims 11 and 16 have been amended in a somewhat similar manner. These features should be readily understood in view of Fig. 1(h) of the present application and the corresponding description thereof, as noted previously above. Applicant respectfully submits that claims 6, 11 and 16 are in compliance with 35 U.S.C. 112, first paragraph, and that this rejection, insofar as it may pertain to the presently pending claims, is improper for at least these reasons.

In the event that this rejection is to be maintained, the Examiner is respectfully requested to clearly establish on the record, by means of various

case law, why claims 6, 11 and 16 would not be considered in compliance with 35 U.S.C. 112, first paragraph in view of Manual of Patent Examining Procedure Section 2163 and *Lockwood v. American Airlines, Inc.*

Claim Rejections-35 U.S.C. 112, second paragraph

Claims 6-9 and 11-19 have been rejected under 35 U.S.C. 112 second paragraph, as being indefinite. The Examiner has asserted that the negative limitations render the claims indefinite as attempting to claim the invention by excluding what the inventor *did not invent*, rather than by distinctly and particularly pointing out what was invented. The Examiner has further asserted that negative limitations must have basis in the original disclosure. This rejection is respectfully traversed for the following reasons.

As asserted on page 8 of the Amendment dated July 22, 2005, contrary to *In re Schechter*, 205 F.2d 185, 98 USPQ 144 (CCPA 1953) as relied upon by the Examiner, *In re Wakefield*, 422 F.2d 897, 899, 904, 164 USPQ 636, 638, 631 (CCPA 1970) as subsequently decided, supports the position that limitations that exclude characteristics of prior art are considered definite (and acceptable), if the recited limitations are definite.

As noted above, claim 6 has been amended to include in combination sidewall spacers "of silicon oxide film formed on the side surfaces of said first and second gates, and not on the side surfaces of said protective layer". Claims 11 and 16 have been

amended in a somewhat similar manner.

Applicant respectfully submits that one of ordinary skill considering the claims in light of the specification, would readily understand and find the claims definite. Particularly, Fig. 1(h) of the present application clearly shows sidewall spacers 37 as formed on gates 35, and not on side surfaces of protective layer 12. Since these negative limitations are clear, the claims must be considered as in compliance with 35 U.S.C. 112, second paragraph. Accordingly, the Examiner is respectfully requested to withdraw this rejection for at least these reasons.

With further regard to this rejection, in the paragraph bridging pages 9 and 10 of the Response to Arguments section of the Final Office Action dated August 9, 2005, the Examiner has asserted with respect to Figs. 1(g) – 1(h) of the present application, that "one having ordinary skill in the art should recognize that forming spacers 37 by etching the oxide layer 35 also results in forming oxide spacers on the edges of the protective layer 12 as well". However, as asserted previously, oxide layer 36 is completely removed from on gate 35 and on substrate 31 by overetching, whereby oxide sidewalls 37 remain only on the sides of gates 35.

If this rejection is to be maintained, the Examiner is respectfully requested to clearly detail on the record, by way of case law, why *In re Wakefield* has not been considered persuasive.

Claim Rejections-35 U.S.C. 102

Claims 6-9, 11-13 and 15 have been rejected under 35 U.S.C. 102(b) as being anticipated by the Hotta reference (U.S. Patent No. 5,418,179). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The semiconductor device of claim 6 includes in combination a field oxide; a protective layer "formed selectively on said field oxide to prevent overetching of said field oxide, said protective layer being a conductive layer and having side surfaces thereof over said field oxide"; and sidewall spacers "of silicon oxide film formed on the side surfaces of said first and second gates, and not on the side surfaces of said protective layer". Applicant respectfully submits that the Hotta reference as relied upon by the Examiner does not disclose these features.

The Examiner has relied upon Fig. 5 of the Hotta reference as disclosing the features of claim 6. However, as described beginning in column 6, line 64 of the Hotta reference with respect to Fig. 5, thick field oxide film 105, n-channel type and p-channel type field effect transistors 106 and 107, and interconnection 119 are covered with an inter-level insulating film 122. One of ordinary skill would readily understand that gate electrodes 111 and 116 in Fig. 5 of the Hotta reference do not have sidewall spacers formed thereon, as would be necessary to meet the features of claim 6. That is, no description is given by the Hotta reference of a structure in which side surfaces of a gate have silicon oxide sidewall spacers thereon, and the silicon oxide has been removed from side surfaces of a protective layer formed on a field oxide so that

sidewall spacers are not thereon. Applicant therefore respectfully submits that the semiconductor device of claim 6 distinguishes over the Hotta reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 6-9, is improper for at least these reasons.

The semiconductor device of claim 11 includes in combination a protective layer "formed on said field oxide to prevent overetching of said field oxide, said protective layer being a conductive layer and having side surfaces thereof over said field oxide"; and sidewall spacers "formed on the side surfaces of said gate, and not on the side surfaces of said protective layer".

As emphasized previously, side surfaces of gate electrodes 111 and 116 in Fig. 5 of the Hotta reference do not include sidewall spacers thereon, as would be necessary to meet the features of claim 11. Accordingly, Applicant respectfully submits that the semiconductor device of claim 11 distinguishes over the Hotta reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 11-13 and 15, is improper for at least somewhat similar reasons as set forth above with respect to claim 6.

Claim Rejections-35 U.S.C. 103

Claims 16-19 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Hotta reference, in view of Applicant's admitted prior art. This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The Examiner has acknowledged that the Hotta reference does not form sidewall spacers on side surfaces of the gate. In order to overcome this acknowledged deficiency, the Examiner has noted that Applicant's admitted prior art Fig. 2(f) teaches a semiconductor device including sidewall spacers 37 formed on side surfaces of gate 35.

Although Fig. 2(h) of Applicant's admitted prior art shows sidewall spacers 37 on gates 35, a protective layer is not formed on field oxide layer 34. Accordingly, neither the Hotta reference nor Applicant's admitted prior art contemplate or provide a structure including in combination a protective layer formed on a field oxide, with sidewall spacers formed on side surfaces of gates and not on side surfaces of the protective layer, so that the previously mentioned problems concerning overetching are avoided. Accordingly, Applicant respectfully submits that the semiconductor device of claim 16 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to claims 16-19, is improper for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present

application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

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